Understanding the LLC Structure in Resonant Applications

Prepared By: Christophe Basso
ON Semiconductor

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The resonant LLC topology, member of the Series Resonant Converters (SRC) begins to be widely used in consumer applications such as LCD TVs or plasma display panels. In these applications, a high level of safety and reliability is required to avoid catastrophic failures once products are shipped and operated in the consumer field. To face these new challenges, ON Semiconductor has recently released to new controllers, the NCP1395 (low−voltage) and the NCP1396 (high−voltage) dedicated to driving resonant power supplies, usually of LLC type. However, before rushing to design a converter of this type, it is important to understand the resonant structure alone, object of the present application note.

The LLC converter

The LLC converter implies the series association of two inductors (*LL*) and one capacitor (*C*). Figure 1 shows a simplified representation of the resonant circuit where:

L_s is the series inductor
L_m is the magnetizing inductor
C_s represents the series capacitor
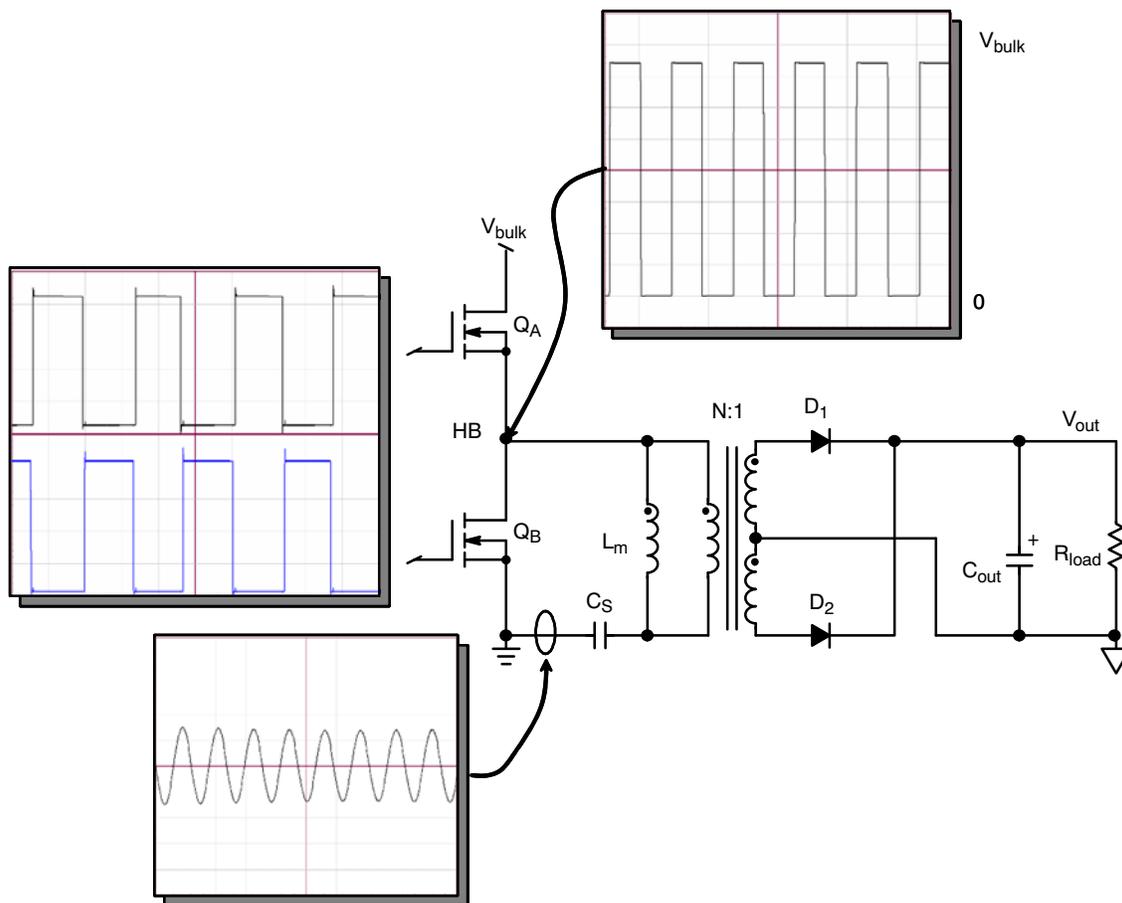
Figure 1. The LLC Topology Uses a Half−Bridge Configuration to Drive the Resonant Circuit

The operating principle is rather simple: a constant 50% duty-cycle switching pattern drives Q_A – Q_B gates and a high-voltage square wave appears on node HB. By adjusting the switching frequency, the controller can control the power flow depending on the output demand. As a transformer is needed for isolation purposes, its magnetizing inductance plays the role of the second inductor L_m. The series inductor, L_s, can either be a separated element or physically lump into the transformer. In this case, a voluntary degradation of both primary and secondary coupling naturally increases the leakage inductance which can act as the series element. There are pros and cons to include the leakage element in the transformer. The cost and the absence of saturation play in favor of the integration but the difficulty to keep a precise value from lots to lots

associated with leaky transformers (radiated noise) has to be kept in mind when selecting the final configuration.

When studying the resonant converter, it is convenient to reduce the architecture to a passive element arrangement such as presented on Figure 2. The high-voltage square signal is replaced by its fundamental content thanks to the first harmonic approximation (the so-called FHA in the literature): because we operate a tuned LC filter, all harmonics can be considered as rejected and only the fundamental passes through. Of course, this statement holds as long the controller drives the resonating work in the vicinity of its resonant frequency. Figure 2 offers such a simplified representation of the resonant cell, actually pointing out a series impedance (L_s and C_s) with a parallel impedance (L_m and the reflected load).
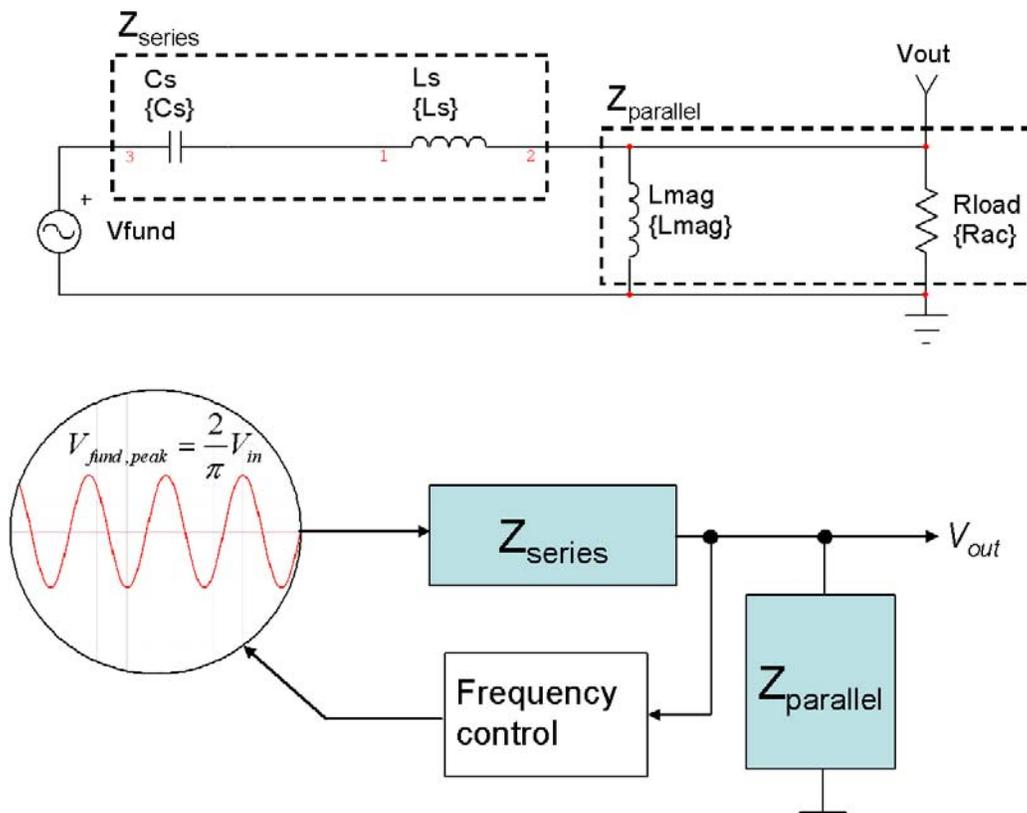
Figure 2. The Impedance Representation Makes the LCC Operation Easier to Understand

Depending on the loading, the network resonant frequency varies between two different values:

- $R_L = 0$, short-circuit, L_m disappears and Z_{series} becomes a short. The series resonant point for Z_{series} is thus

$$F_{max} = F_S = \frac{1}{2\pi \sqrt{L_S C_S}}$$

(eq. 1)

At $F_{sw} = F_S$, Z_{series} becomes a short and the ac transfer function drops to 1 or 0 dB.

- $R_L = \infty$, light or no load condition, L_m appears in series with L_s and the whole network resonates to

$$F_{min} = \frac{1}{2\pi \sqrt{(L_S + L_m)C_S}}$$

(eq. 2)

- $0 < R_L < \infty$, the resonance which combines L_m and L_s, shifts depending on the total quality coefficient.
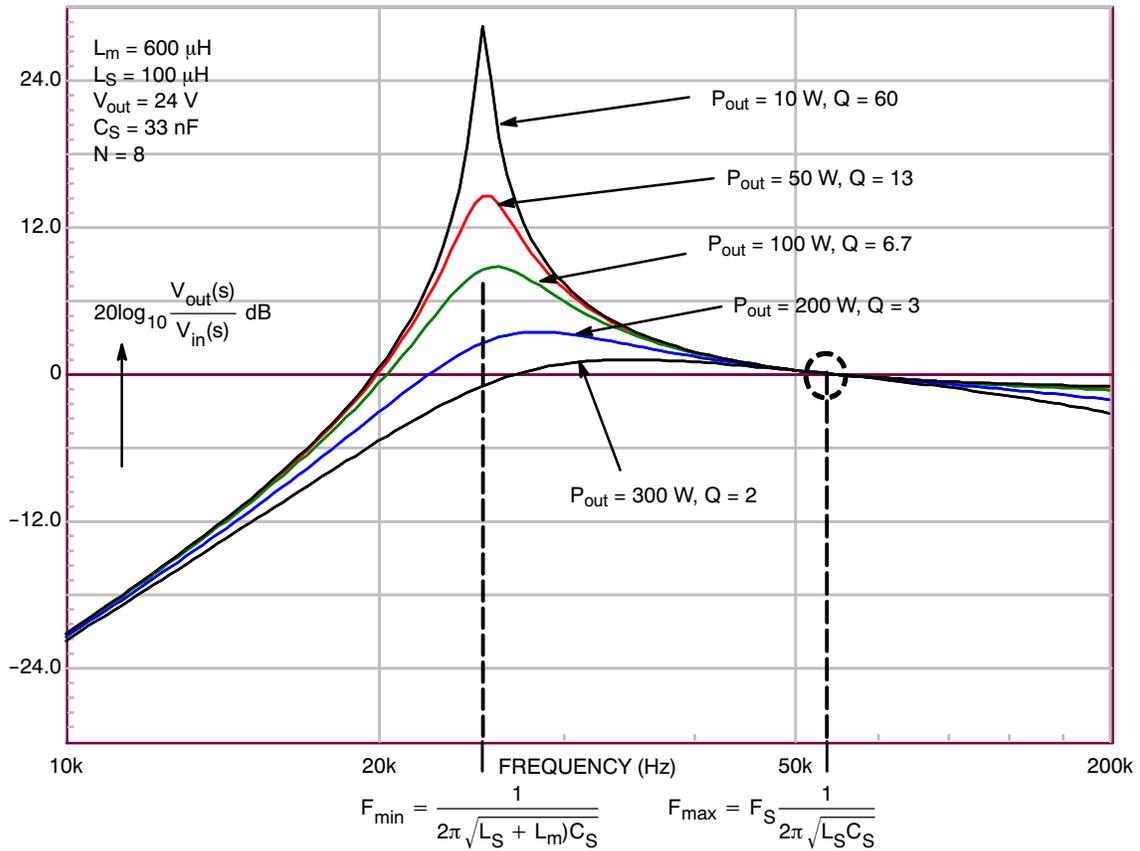
Figure 3. The AC Response of Figure 2 Circuit with Various Load Conditions

This is actually what Figure 3 plots suggest by showing the ac transfer function of Figure 2 as the load changes.

If we now study the impedance seen from the half−bridge node, we have an expression showing a series association of inductors and a capacitor. Sticking to Figure 2 sketch and writing the impedance seen between ground and Node 3, we have:

$$Z_{in} = Z_{L_S} + Z_{C_S} + Z_{L_{in}} \| R_{ac} \qquad \text{(eq. 3)}$$

$$Z_{in} = \left[\frac{(\omega L_m)^4 R_{ac}^2}{(R_{ac}^2 + \omega^2 L_m^2)^2} + \left(\omega L_S - \frac{1}{\omega C_S} + \omega L_m \frac{R_{ac}^2}{R_{ac}^2 + \omega^2 L_m^2} \right)^2 \right]^2 \qquad \text{(eq. 4)}$$

In the low frequency portion, the terms associated with inductors are of less importance and C_S dominates. The impedance is thus capacitive. As the frequency increases, the inductive portion starts to kick−in and the impedance goes up. This is what Figure 4 describes. As one can see, all the curves go through point A whose value is independent from the resistive loading. For the sake of a friendly exercise, we can solve Equation 4 with two different R_{ac} values and find the frequency at which input impedances equal. We obtain:

$$\omega_A = \sqrt{\frac{2}{L_m C_S + 2 L_S C_S}} \qquad \text{(eq. 5)}$$

If we substitute this value into Equation 4, the impedance at point A is:

$$Z_A = \frac{\frac{L_m}{2 L_S} L_S \omega_S}{\sqrt{\frac{L_m}{2 L_S} + 1}} \qquad \text{(eq. 6)}$$

If we define the ratio R by L_m/L_S, we can re−arrange equation 6:

$$Z_A = \frac{R}{\sqrt{2(R + 2)}} \sqrt{\frac{L_S}{C_S}} = \frac{R}{\sqrt{2(R + 2)}} Z_O \qquad \text{(eq. 7)}$$

Where Z_0 represents the characteristic impedance of the series resonant network. Using the numerical values noted in the graphs, we obtain a frequency of 43.8 kHz and an impedance of 38.3 dBΩ (82.6 Ω).
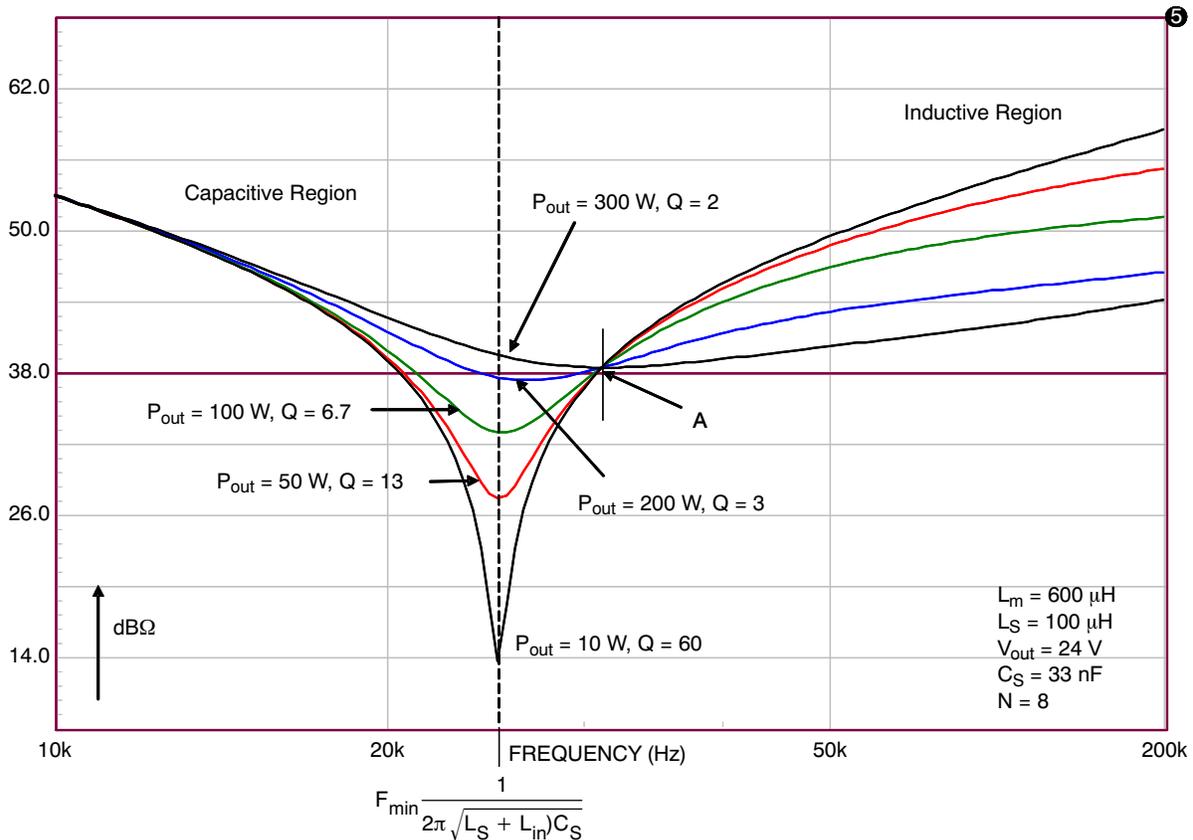
Figure 4. Impedance Plots at Various Power Levels

If we now observe the resonant current waveforms in a LLC converter working below or above the series resonance F_s, we have different types of operation:

- Capacitive mode: in this mode, where the current leads the voltage, the bridge MOSFETs operate in zero current switching (ZCS). ZCS means that power MOSFETs are turned–off at zero current. Back to figure 3, we can see that the output level goes up as the frequency increases.

- Inductive mode: in this mode, the current lags the voltage and the power switches are turned–on at zero volt (ZVS), virtually eliminating all capacitive losses. This operating way implies that a certain delay exists before operating the concerned MOSFET so that its

body diode turns on first. Observing figure 3, the output level goes down as the frequency increases.

Most of the LLC converters operate in the inductive region for the second bullet reason. Also, given the feedback polarity, if by mistake the closed–loop LLC enters the left side of the resonance, the control law reverses and a power runaway obviously occurs. It is thus extremely important to clamp down the lower frequency excursion in fault condition or during the startup sequence to avoid falling on the other slope of the characteristics.

The inductive region can be split into two other regions, depending where you operate compared to the resonant series frequency F_s, as defined by Equation 1. Figure 5 represents the classical set of curves often found in the dedicated literature:
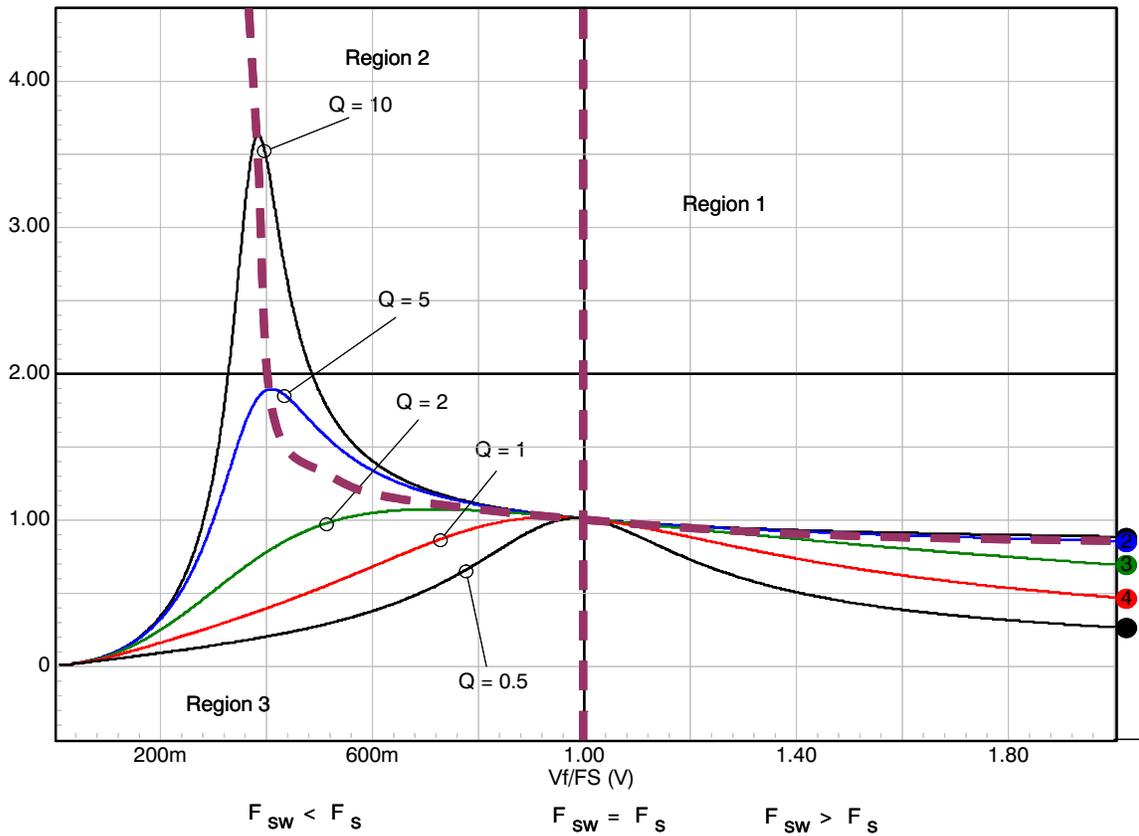
Figure 5. Typical Transmittance Curves with Various Loading Conditions, Highlighting Three Distinct Regions

Region 3 is the capacitive mode where you do not want to operate since ZVS is a wanted feature for the power switches. In regions 1 and 2, you still have ZVS on the power MOSFET's and the output diodes are operated in Zero Current Switching (ZCS), cancelling all associated losses at turn–off. Before discussing the benefits of a particular solution, let us have a look at the various operating phases the LLC converter is made of.

Operating Waveforms Below the Series Resonance, $F_{sw} < F_s$

For this example, we have selected a set of elements which operate the converter below the series resonance defined by Equation 1. The following value have been used:

$L_m = 700 \ \mu H$
$L_s = 116 \ \mu H$
$C_s = 28 \ nF$
$N = 8$

$$F_{max} = F_S = \frac{1}{2\pi \sqrt{L_S C_S}} = \frac{1}{6.28 \times \sqrt{116\mu \times 28n}}$$

$$= 88.3 \ kHz$$

$$F_{min} = \frac{1}{2\pi \sqrt{(L_S + L_m)C_S}}$$

$$= \frac{1}{6.28 \times \sqrt{(116\mu + 700\mu) \times 28n}} = 33 \ kHz$$

$F_{sw} = 70$ kHz at full load and nominal input voltage.

The converter delivers 24 V@10 A from a 380 Vdc input source and a simulation has been performed using the above values. Figure 6 shows the main waveforms obtained from the simulator. Let us study the switching events step by step to learn about the LLC behavior in this region.
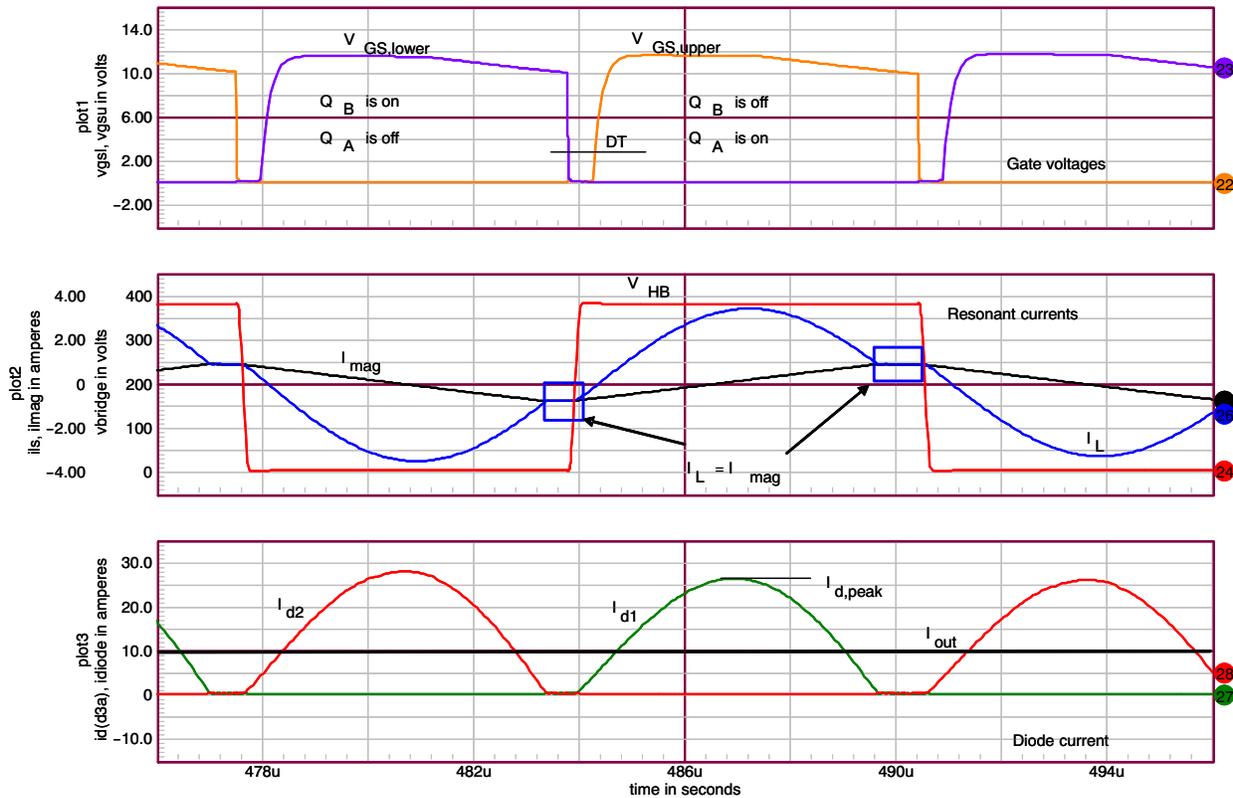
Figure 6. Waveforms Obtained for a Converter Operated Below the Series Resonant Frequency

Q_A is off, Q_B is on, D_2 is conducting :

The low–side MOSFET Q_B imposes a 0 V potential on the half–bridge node and the current circulates from its drain to source (first quadrant). The upper parasitic capacitor C_{ossA} is fully charged to the input voltage V_{bulk} since the HB node is grounded by Q_B. The secondary diode D_2 is conducting and imposes a voltage reflection $-NV_{out}$ over the magnetizing inductor L_m. Its current linearly decreases with a slope of $-NV_{out}/L_{in}$. As this inductor is dynamically shorted by the voltage reflection, it does not participate to the on–going resonance between L_s and C_s which deliver the output energy (the input source is out of the picture). The current flowing into the transformer primary side (given its theoretical representation, L_m associated to a perfect transformer) is the main current I_L minus the magnetizing current I_{mag}. D_1 is blocked and undergoes twice the output voltage given the transformer coupling. The circuit resonates to F_s as L_m is shorted. Figure 7 depicts the situation during this period of time.

Q_A is off, Q_B is on, D_2 turns off:

As the network current I_L resonates in a sinusoidal manner, its amplitude peaks and then starts to dip towards 0. When it reaches a level equal to that of the magnetizing current, no current circulates in the transformer anymore: D_2 blocks and the voltage reflection over L_m disappears. The magnetizing inductor now comes back in series with L_s and C_s and changes the resonant frequency from F_s to F_{min}: the LLC converter is really a multi–resonant structure and the plateau – actually a small arch of a lower sinewave oscillation – in the current as it appears on figure 6 testifies for it. Both diodes are now blocked and this moment lasts until Q_B opens. Figure 8 represents the circuit during this time. As one can see, the output capacitor alone supplies the energy to the load.
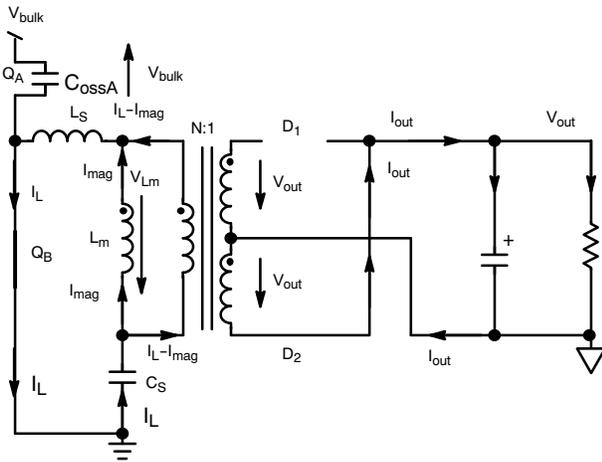
Figure 7. Q_A is Off, Q_B is On and Diode D_2 Conducts Current. L_m is Off the Picture as it is Dynamically Shorted by the Output Voltage Reflection.
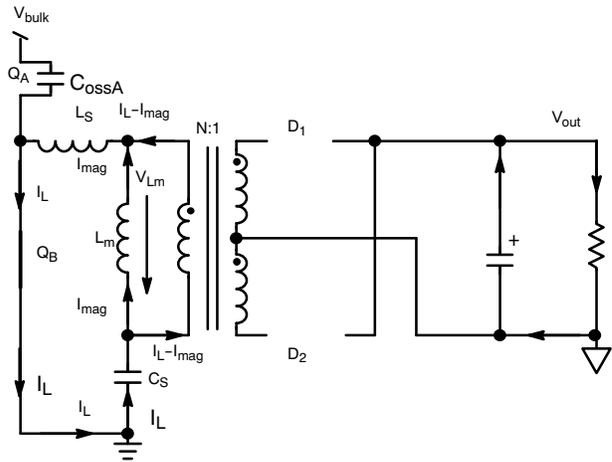
Figure 8. Q_A is Off, Q_B is On and Diode D_2 Blocked. L_m Comes Back Again in the Resonating Network and Changes the Resonant Frequency to F_{min}.

Q_A is off, Q_B is Off, Both Secondary Diodes are Blocked

Both transistors are now open, this is the dead–time period (DT on Figure 6). The dead–time is placed here to avoid cross–conduction between both MOSFETs but also to favor Zero Voltage Switching as we will see in a moment. Because the current was circulating from drain to source in Q_B, the circuit no longer sees an ohmic path when this transistor opens. The current strives to find a way through the parasitic drain–source capacitors C_{oss} of both Q_A and Q_B: C_{ossB} starts to charge (it was previously discharged by Q_B being on) and given the rise of V_{HB} towards the high voltage rail, C_{ossA} sees its terminals voltage going down to zero and then

reversing (Figure 9). At this moment, when the HB node reaches $V_{bulk} + V_f$, the body–diode of Q_A conducts and ensures energy re–cycling through the input source (Figure 10). You understand that this dead–time period must last a time long enough to allow for the complete discharge of C_{ossA} before re–activating Q_A so that its body–diode turns on first. If not, hard switching occurs and efficiency suffers.

As currents are oscillating, a time is reached where I_L and I_{mag} are no longer equal (end of the plateau) and a current circulates again in the primary side. D_1 starts to conduct and NV_{out} appears across L_m: the resonant frequency goes back from F_s to F_{min}. Figure 10 describes this moment.
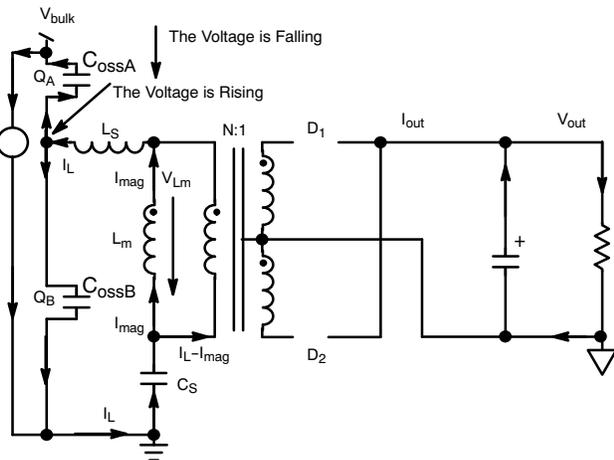
Figure 9. Q_A is Off, Q_B is Off. The Current Finds a Circulating Path Through Both Transistors C_{oss}, Both Secondary–Side Diodes are Off.
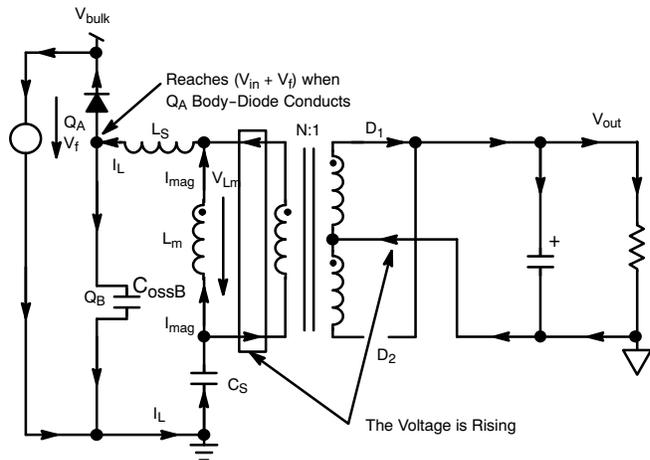
Figure 10. Q_A and Q_B are Still Off. The Current Finds a Circulating Path through the Upper–side Body Diode. D1 Starts Conducting at the End of the Plateau when $I_L \neq I_{mag}$.

Q_A is on, Q_B is off, D_1 is on

Now that Q_A body–diode is conducting, we have a negligible voltage across its drain and source terminals: we

can therefore safely turn it on and benefit from Zero Voltage Conditions. As we have a sinusoidal waveform in the network, the resonating current reaches zero and reverses.

L_m is still dynamically shorted as D_1 is conducting. The energy is delivered by the source to the output load. This is illustrated by Figure 11.

Q_A is on, Q_B is off, D_1 turns off

The current I_L is moving down and reaches the magnetizing current level, we are the second plateau on

Figure 6. At this point, no current circulates in the transformer and D_1 naturally blocks. As explained before, the magnetizing inductor re-appears in the circuit since the output voltage reflection is gone. The resonant frequency changes from F_{min} to F_s and the energy to the load is delivered by the output capacitor alone. Figure 12 shows the circuit state during this event.

Figure 11. The Current is Now Flowing from the Source to the Output Via the Upper–Side Transistor Q_A.
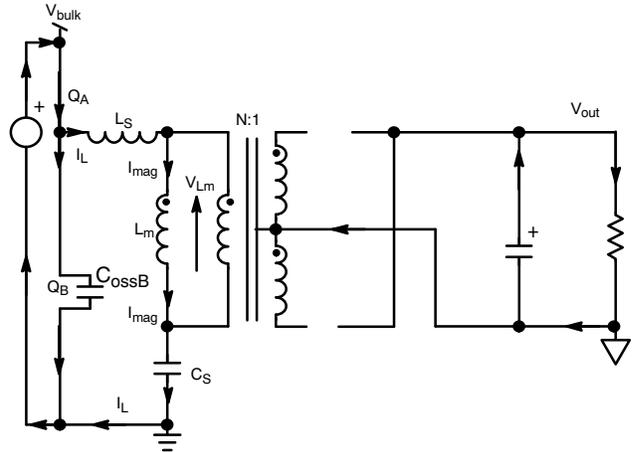
Figure 12. As Both Diodes are Off, the Network Includes the Magnetizing Inductance which Changes the Resonant Frequency.

QA is of, QB is off, both secondary diodes are blocked

At a certain time, both transistors block and only their drain–source capacitors remain in the circuit. The current keeps circulating in the same direction but C_{ossA} starts to charge: the voltage on the HB node drops and C_{ossB} depletes

towards ground. The drain falls down in a resonating manner, involving both C_{oss} in parallel and the equivalent inductor made of $L_s + L_m$. Figure 13 represents the circuit during this event.
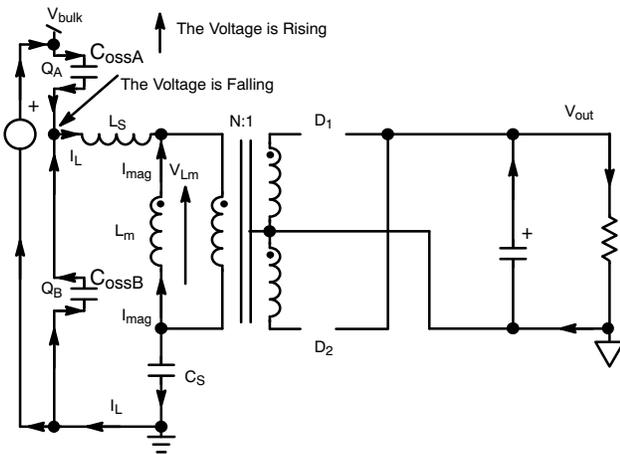
Figure 13. The Current is Still Flowing through the Source and Contributes to Discharge C_{ossB}.

Figure 14. When the Voltage on the Node HB Swings Below Ground, Q_B Body–Diode Conducts.

The bridge voltage further dips and becomes negative until the body-diode of Q_B conducts. This is what Figure 14 suggests. At the end of the plateau, where $I_L = I_{mag}$, D_2 will start conducting, reflecting $-NV_{out}$ over the primary inductance. The energy comes from C_s and L_s, as the source

is not playing any role here. The controller now activates Q_B in ZVS and the transistor conducts in its 3rd quadrant for a few moments, until the current reaches zero and swings negative: we are back at the beginning of the first phase.

Zero Voltage Switching

Figure 15 zooms on these ZVS events and show the various signals in play. The MOSFET current starts to be negative before the appearance of its gate-source bias: this is the body-diode conduction period. Then the MOSFET turns-on at a V_f across its drain-source terminals but the current is still negative: we are in the 3rd quadrant conduction. Finally, the current becomes positive and flows from drain to source, back to the 1st quadrant.
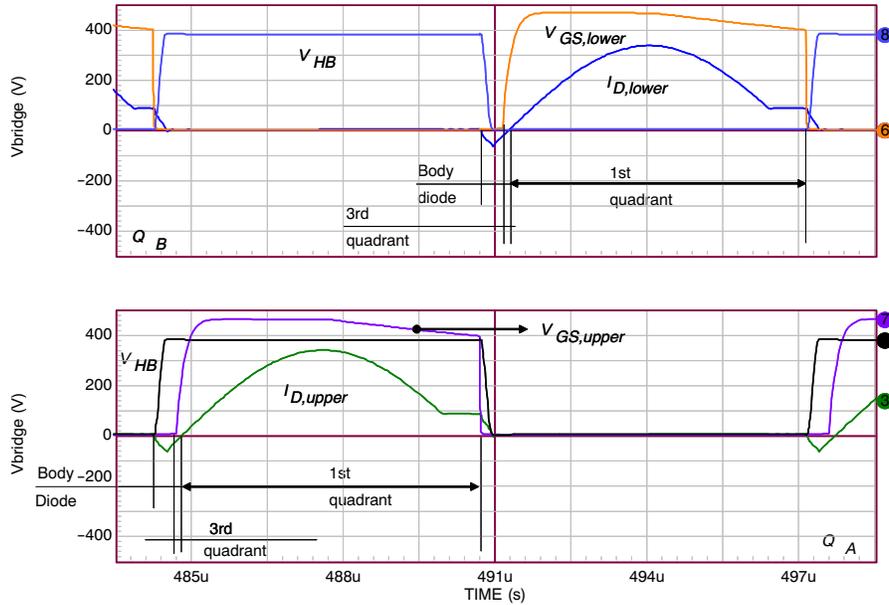
Figure 15. Simulation Results Zooming on the MOSFET Variables
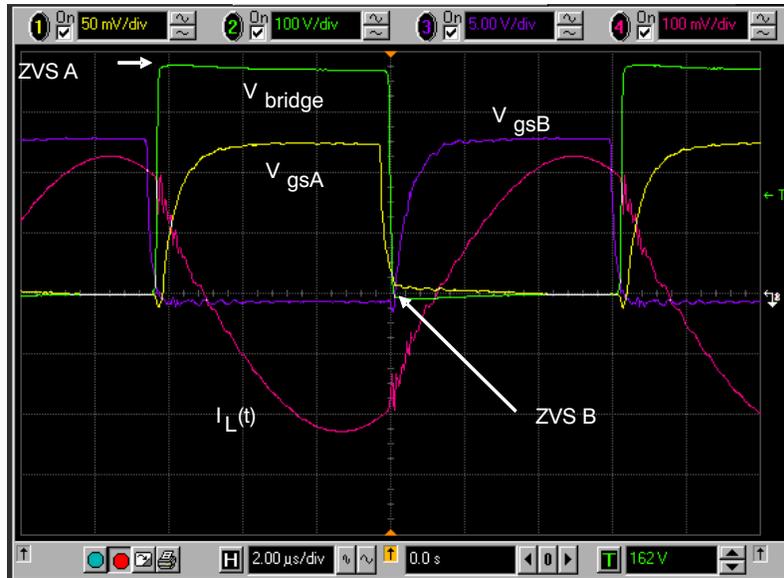
Figure 16. Measured Signals on a Demonstration Board Showing the ZVS Operation on Q_A.

The selection of a controller where the dead-time is adjustable therefore represents an important selection argument to fine tune the behavior and ensure a minimum conduction period of both body-diodes.

Zero Current Switching

By the term ZCS, we assume a natural blocking event when the current in the semiconductor is zero. When operating the LLC converter below F_s, as it is the case in this

example, both secondary–side diodes are operated in ZCS. The current in the concerned diode (D_1 or D_2) naturally reaches 0 when the magnetizing current I_{mag} equals the main resonating current I_L. This is the plateau on figure 6. Observing the diode current in this particular mode gives smooth signals as shown on Figure 17.
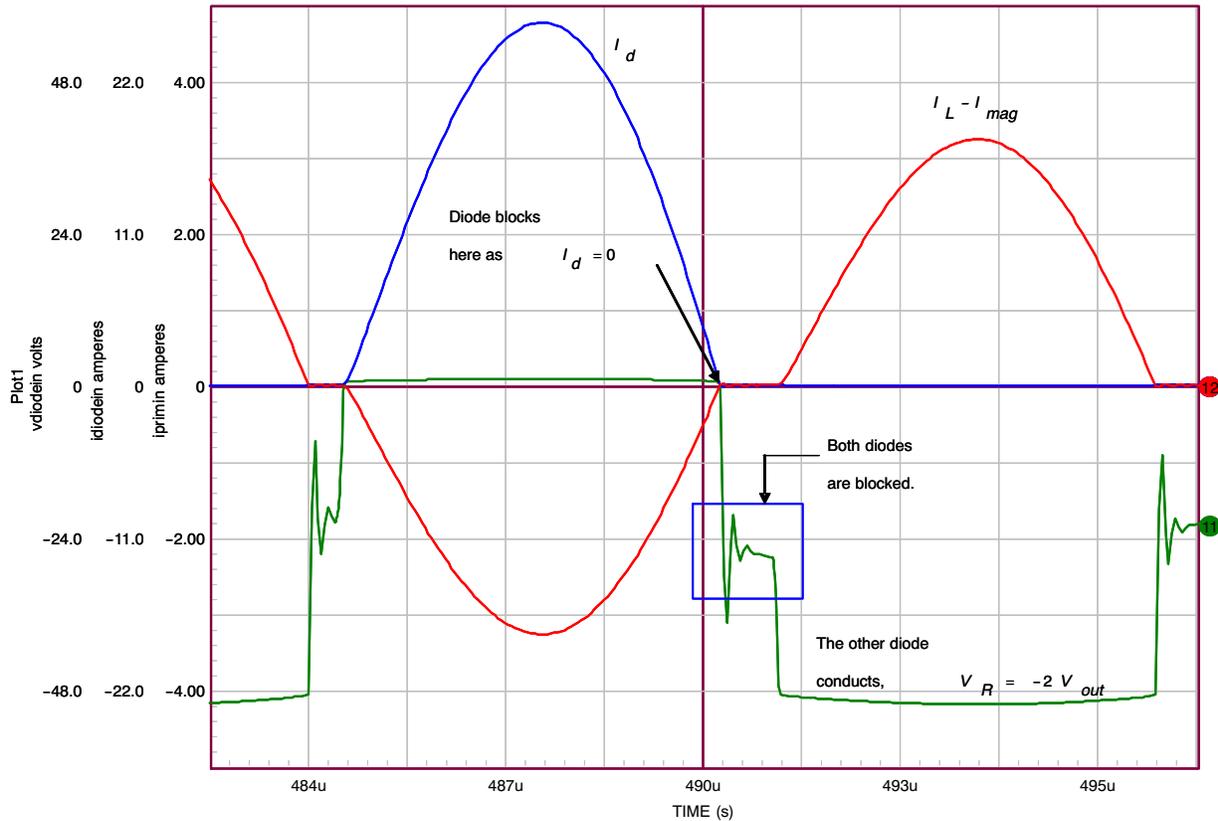
Figure 17. The Secondary–Side Diodes are Naturally Blocked When the Primary Current Vanishes to Zero

Startup sequence and short–circuit

During startup or short–circuit, the magnetizing inductor is shorted and the resonant frequency becomes F_s. Because we designed the LLC converter to operate at a frequency lower than F_s, the operating fault mode (lack of feedback) of the controller naturally lies below F_s. In other words, if the LLC converter quickly starts–up, without soft–start at all, the controller will quickly sweep from a high frequency value down to the minimum authorized in case of fault. The current in the network can therefore peak to a high value (at resonance, the LC impedance is only limited by ohmic losses) and destroy the power MOSFETs instantaneously. Figure 18a shows an oscilloscope shot captured on a LLC circuit started with a short soft–start period ($\approx$20 ms): the current peaks to 6 A. Increasing the soft–start period to a few hundred of milliseconds clearly helps to smooth the peak and keep it below 4 A.

Short–circuit protection is more difficult to achieve given the resonating nature of the circuit. Some solutions exist like differentiating the voltage across the capacitor C_s and routing the resulting voltage to a fast latch input. Figure 19 shows this solution where the component values must be adjusted to avoid false triggering in normal operating transients.

Reference [1] has experimented a solution where the resonating capacitor is split in two values – $C_s/2$ – and two high voltage diodes clamp the voltage excursion between ground and the bulk rail. As the voltage across the capacitor is limited, the resonant current is also clamped. The solution appears in Figure 20. There are several drawbacks associated to the usage of this diode arrangement such as a variable clamping level in relationship to the high–voltage rail. However, experience shows that this simple circuit brings an efficient protection to the converter experiencing a short–circuit. The diodes must be of fast types, MUR260 can be selected for this purpose.

a

b
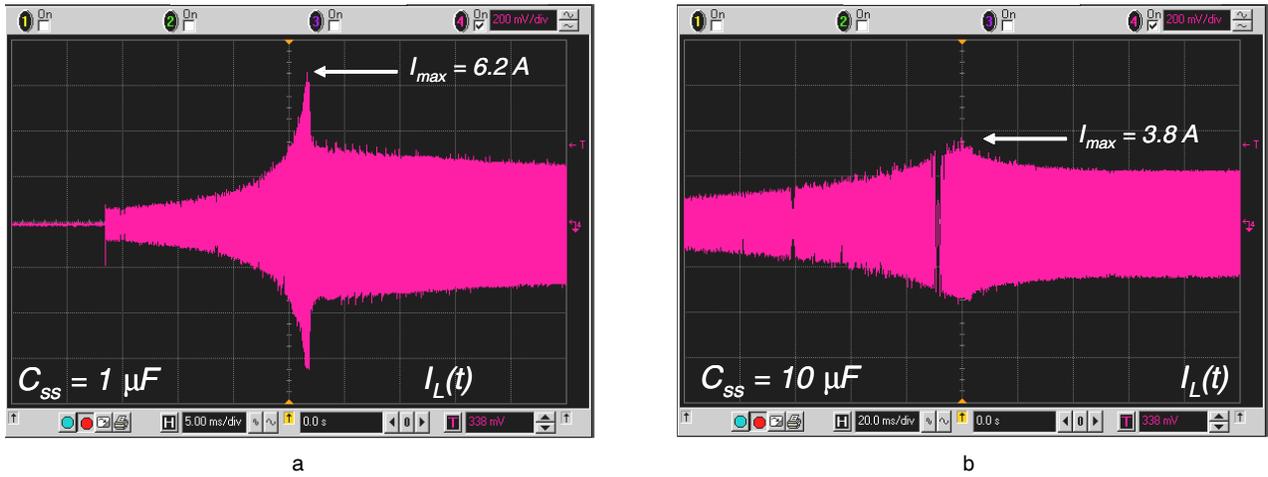
Figure 18. The LLC converter peaks to a high current if started too quickly. Increasing the soft–start sequence naturally calms down the current excursion.
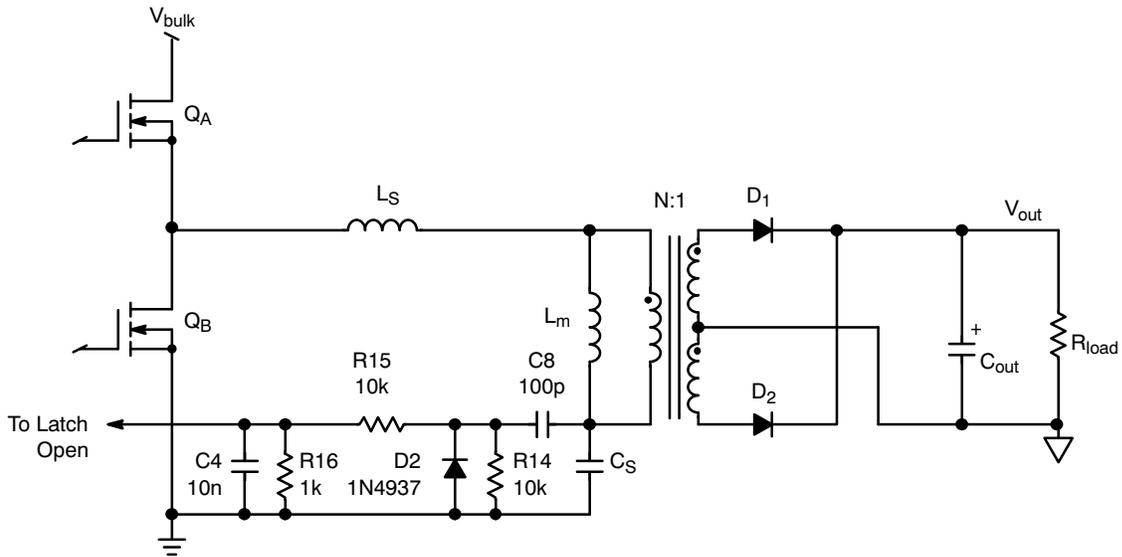
Figure 19. Differentiating the Voltage Across the Resonant Capacitor Gives an Indication of the Current Flowing Through it
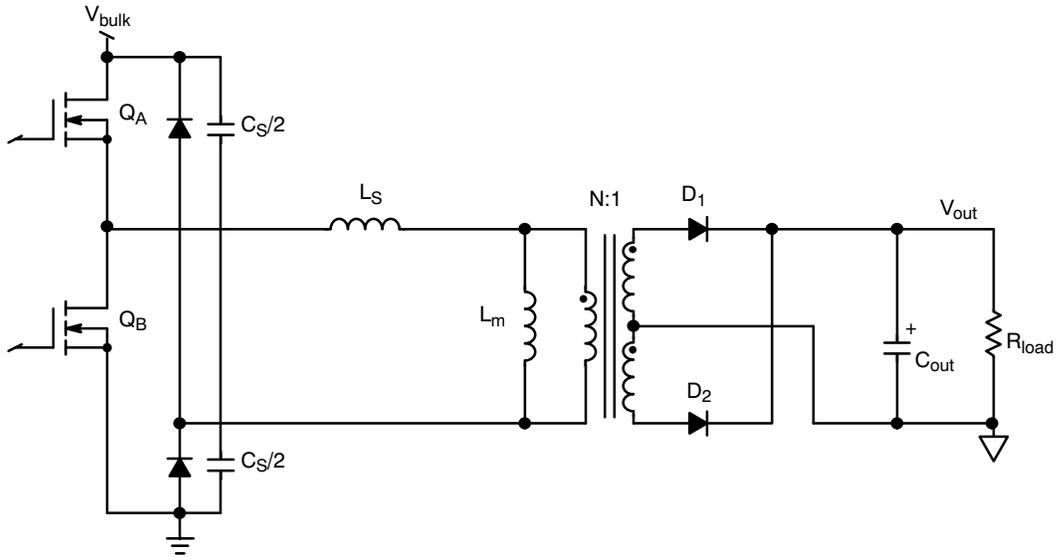
Figure 20. To Keep the Voltage Excursion on the Resonant Capacitor within Safe Limits, a Diode Network Forbids any Lethal Runaways

Operating Waveforms Above the Series Resonance, $F_{sw} > F_s$

For this example, we have selected a set of elements which operate the converter above the series resonance defined by equation 1. The following values have been used:

L_m = 1.2 mH
L_s = 200 μH
C_s = 44 nF
N = 6

$$F_{max} = F_S = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{6.28 \times \sqrt{200\mu \times 44n}}$$

$$= 53.7 \text{ kHz}$$

$$F_{min} = \frac{1}{2\pi\sqrt{(L_S + L_m)C_S}}$$

$$= \frac{1}{6.28 \times \sqrt{(200\mu + 1.2m) \times 44n}} = 20 \text{ kHz}$$

F_{sw} = 70 kHz at full load and nominal input voltage.

The converter still delivers 24 V@10 A from a 380 Vdc input source and a simulation has been conducted using the above values. Figure 21 shows the main waveforms obtained from the simulator. There are several differences between this operating mode and the previous one:

1. In the previous mode, the magnetizing inductance was released at a point where both secondary-side diodes were blocked ($I_L = I_{mag}$). The resonant frequency was therefore moved from F_s to F_{min} during a certain time (the plateau on Figure 6). When operated above the series frequency F_s, the magnetizing inductance is always shorted by the reflected voltage NV_{out} or $-NV_{out}$ as one of the

secondary diode is always conducting. In other words, a single resonance occurs in this mode at full power, implying L_s and C_s only. L_m is out of the picture as long as the converter operates in continuous conduction mode (full load operation).

2. Observing Figure 21, we can see that the main resonant current I_L changes from a sinusoidal waveshape to a straight line, implying a change in the operating mode. This change occurs when a voltage discontinuity appears across L_s terminals. This discontinuity comes from the delay between the bridge signal V_{HB} and the reflected voltage polarity across the magnetizing inductor L_m. Figure 22 zooms on this particular moment where we can see that the bridge voltage goes down to zero via the body-diode activation of Q_B, but because there is still current flowing in the transformer primary side (I_L is different than I_{mag}), one of the secondary diode is still conducting, imposing a constant reflected output voltage across L_m. The voltage across L_s is up by one step which starts to reset it towards zero. This is the beginning of the linear segment, if we consider the voltage across L_s almost constant. When I_L reaches the magnetizing current I_{mag}, the conducting diode blocks and the primary current transitions to the second diode which now conducts. The voltage polarity across L_m reverses and the resonant current goes back to its sinusoidal shape. The next segment occurs when Q_B opens and the bridge voltage jumps to V_{in} via Q_A body-diode. This segment lasts until I_L reaches I_{mag} again.
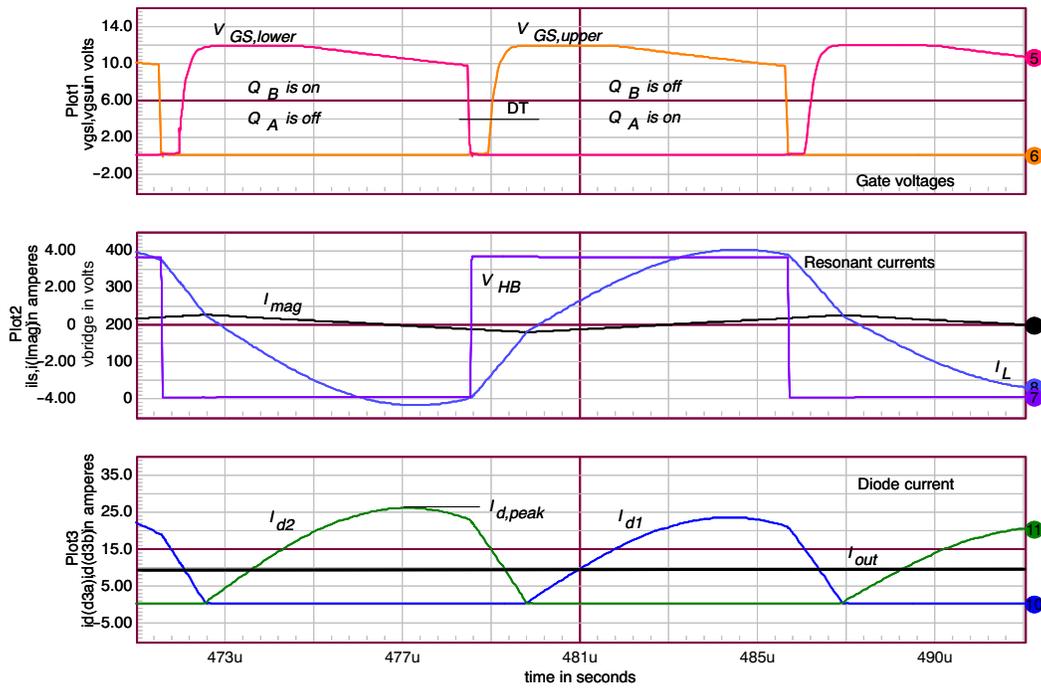
Figure 21. Figure 6 Waveforms Updated with a Converter now Operating Above the Series–Resonant Frequency F$_s$
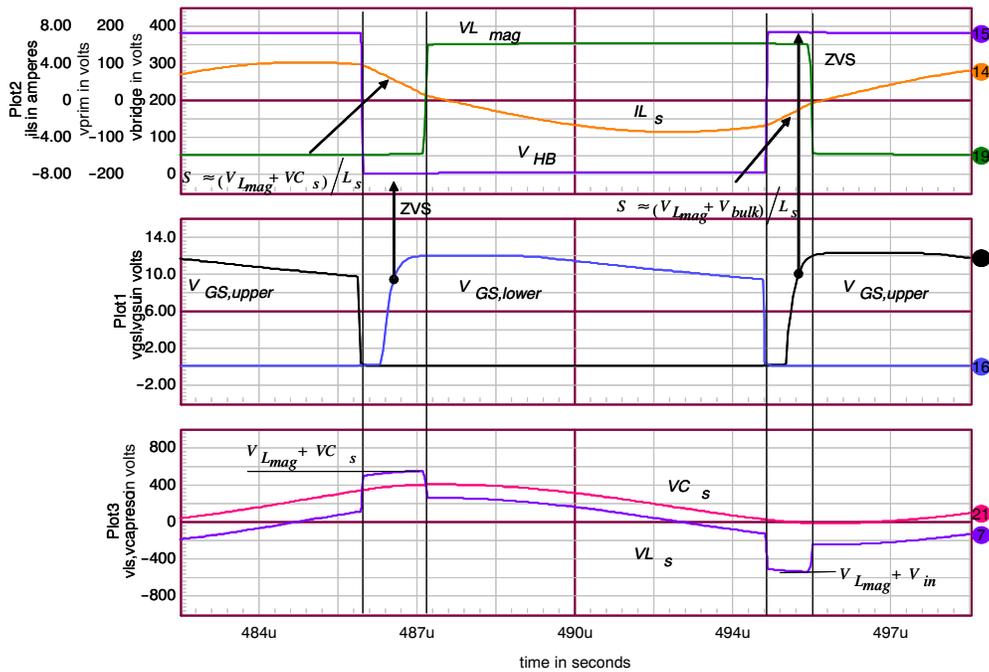
Figure 22. The Voltage Discontinuity Across Ls Induces a Linear Segment in the Resonant Waveform

1. The diode are still operated in ZCS despite a switching frequency above F$_s$. This is thanks to the linear reset taking place on the resonant current (the segment on I$_L$(t)) which smoothly leads the concerned diode to a blocking state. Figure 23 illustrates this fact.
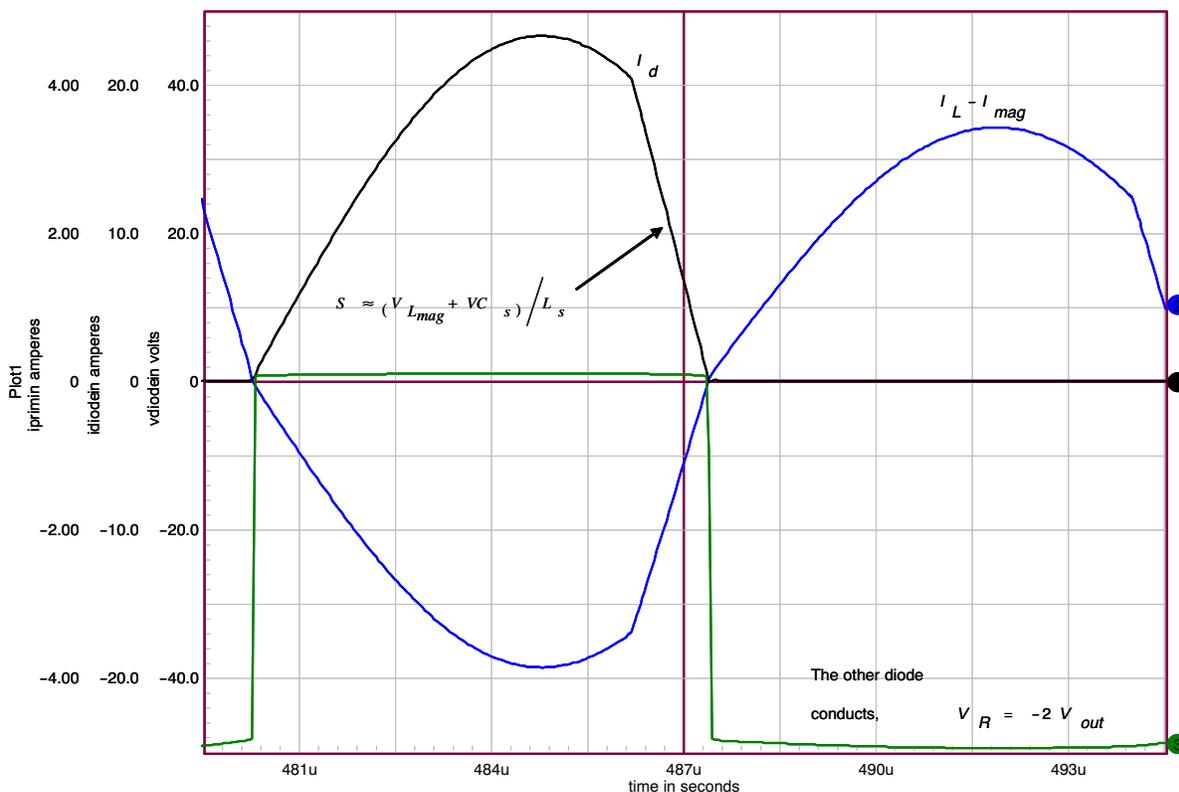
Figure 23. A Zoom on the Switching Diodes Reveal a ZCS Operation for F_{sw} greater than F_s

Operating Waveforms at the Series Resonance, $F_{sw} = F_s$

For this final example, we have selected a set of elements which operate the converter at the series resonance defined by Equation 1. The following values have been used:

L_m = 1.6 mH
L_s = 277 μH
C_s = 17 nF
N = 8

$$F_{max} = F_S = \frac{1}{2\pi \sqrt{L_S C_S}} = \frac{1}{6.28 \times \sqrt{277\mu \times 17n}}$$

$$= 73.4 \text{ kHz}$$

$$F_{min} = \frac{1}{2\pi \sqrt{(L_S + L_m)C_S}}$$

$$= \frac{1}{6.28 \times \sqrt{(277\mu + 1.6m) \times 44n}} = 28.2 \text{ kHz}$$

F_{sw} = 73 kHz at full load and nominal input voltage.

When operated at the tank resonant frequency, the main current $I_L(t)$ is sinusoidal as confirmed by Figure 24.
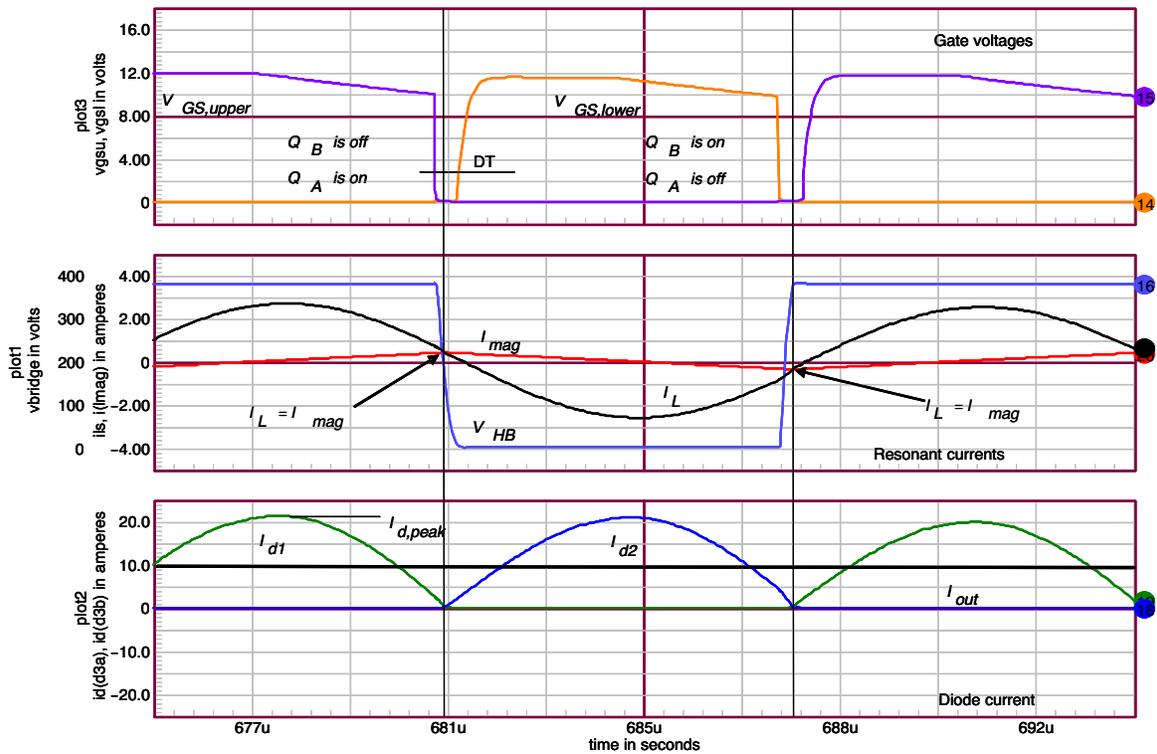
Figure 24. At the Resonant Frequency, the Main Current is Sinusoidal. Also, There is no Deadtime Between the Secondary−Side Diode Conduction Periods.

In this mode, the EMI signature is excellent as the distortion is least compared to the other modes. The secondary−side currents are at the boundary between the segment-like shape and the dead-time period, as respectively observed for $F_{sw} > F_s$ and $F_{sw} < F_s$. As we observed before, the diode block when the resonant current equal the magnetizing current I_{mag}.

Operating the LLC at the series resonant frequency offers another advantage. Back to Figure 3, we can see a point where all curves cross. This point, for which $V_{out}/V_{in} = 1$, is reached at the series resonance. When operated at this particular position, the LLC resonant network transfer function becomes insensitive to load variations. This characteristics is sometimes exploited when a LLC converter is designed to operate at a fixed switching frequency locked to F_s and the feedback loop drives the output voltage of a pre-converter.

The RMS current in the output capacitor is also at its lowest value as no discontinuity, or deadtime, exists as shown on figure 6 for $F_{sw} < F_s$. We can quickly derive its value in presence of sinusoidal signals:

$$I_{d.RMS} = \frac{I_{d.peak}}{\sqrt{2}} \qquad (eq.\ 8)$$

The total dc current contributed by both diodes in the output current delivered by the converter. This dc current can be linked to the equivalent full-wave rectification and equals:

$$I_{dc} = \frac{2I_{d.peak}}{\pi} \qquad (eq.\ 9)$$

We can then evaluate the ac current flowing into the output capacitor applying the following equation:

$$I_{Cou.RMS} = \sqrt{I_{RMS}^2 - I_{dc}^2} = \sqrt{\frac{I_{peak}^2}{2} - \frac{4I_{d.peak}^2}{\pi^2}} \approx 0.3\ I_{d.peak} \qquad (eq.\ 10)$$

In the simulated example, if we have a diode peak current of 15.7 A at steady-state, the RMS current flowing in the capacitor is therefore 4.7 A. If we simulate a similar converter in a 100 kHz 2-switch forward configuration, the RMS current in the output capacitor reduces down to 0.5 Arms. That is one of the major disadvantage of the resonant operation. The switching losses are almost removed, allowing high-frequency operation, but conduction losses increase significantly.

Conclusion

This quick study of the LLC converter explores the various operating modes of the power supply, mainly dictated by the switching frequency value in relationship to the series resonant frequency F_s. Most of LLC designs are operated at the series resonance in full load and nominal input voltage conditions. The controller allows operation below F_s during an input voltage drop and lets the frequency exceed F_s in light load conditions. Despite sinusoidal

currents, care must be taken in the selection of the output capacitor given the high ac ripple. Compared to buck−derived applications, this is the penalty to pay with LLC converters, however, largely compensated by the reduction in switching losses on both the primary transistors (ZVS) and the secondary−side diodes (ZCS).

References:

1. Bo Yang, Fred C. Lee, Matthew Concannon, Over Current Protection Methods for LLC Resonant Converter, IEEE Conference 2003

2. Bo Yang, "Topology Investigation for Front−End dc−dc Power Conversion for Distributed Power System", Virginia Tech Dissertation, 2003" http://scholar.lib.vt.edu/theses/available/etd−09152 003−180228/unrestricted/